Variable Gain Operational Amplifier

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Design Requirements

Updated specifications and gain-dependent input limit

Parameter	Target
Supply / power	1.2 V / < 5 mW
Gain range / step	−6 to +18 dB / ≤ 3 dB
Bandwidth / gain error	> 250 MHz at all gains / < 1.5 dB
Linear output swing	≥ 300 mVpp
THD	< −35 dB at 25 MHz, 250 mVpp output
Input-referred noise	< 15 nV/√Hz at 25 MHz and maximum gain

First Iteration

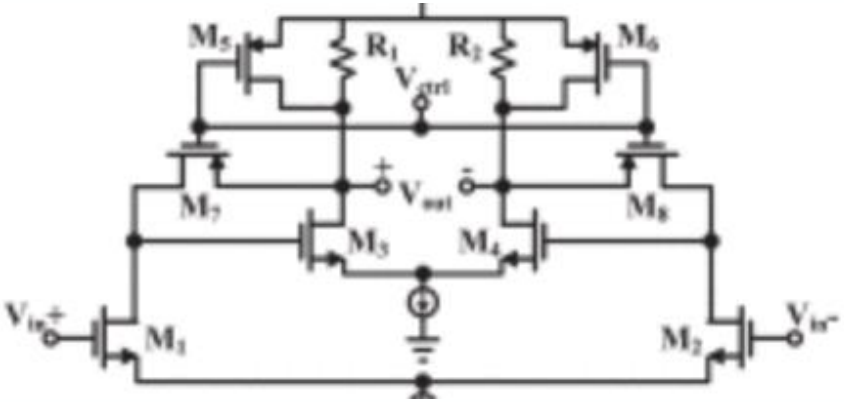


Fig I

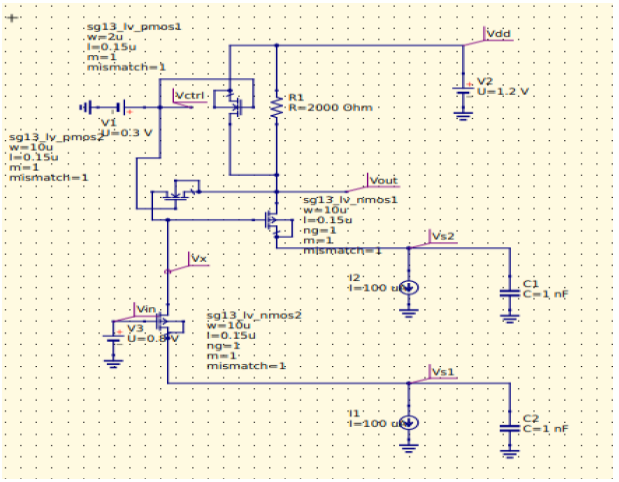


Fig II

- Figure I shows a conventional cherry hopper topology
- Figure II shows a one-sided cherry hopper topology

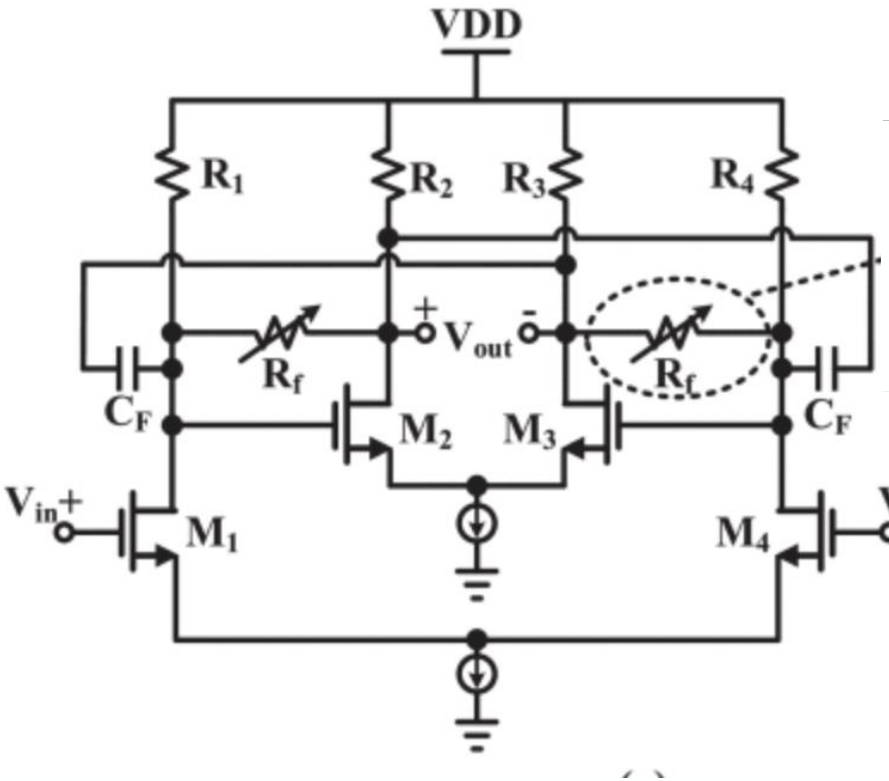
Originally chose a conventional cherry hopper that I made into a single ended design.

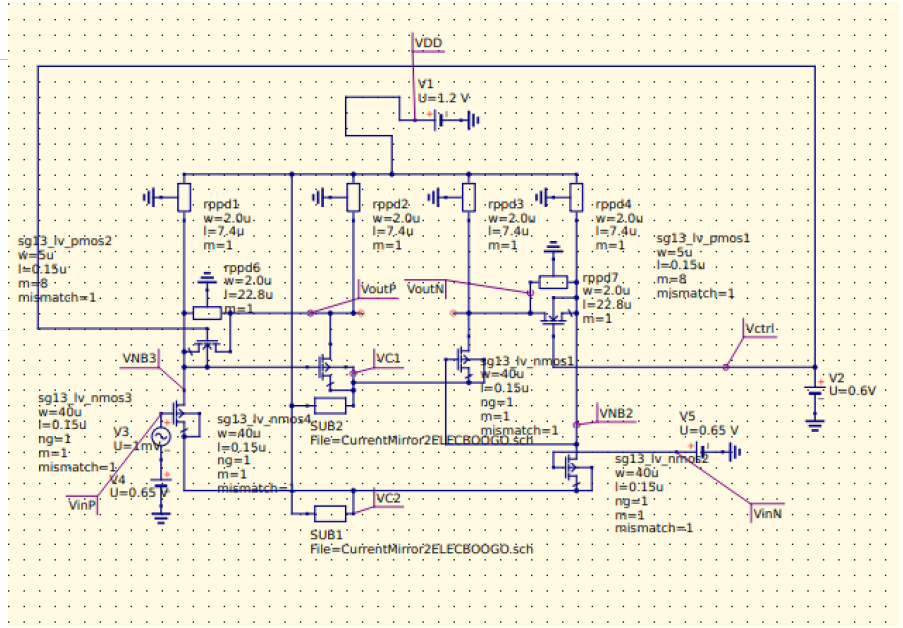
Had Issues with getting gain levels to work and chaining cells gave bandwidth errors.

Source: C. Fan et al., "Design of a Wideband dB-Linear Variable Gain Amplifier," IEEE Access, 2021.

Final Design Choice

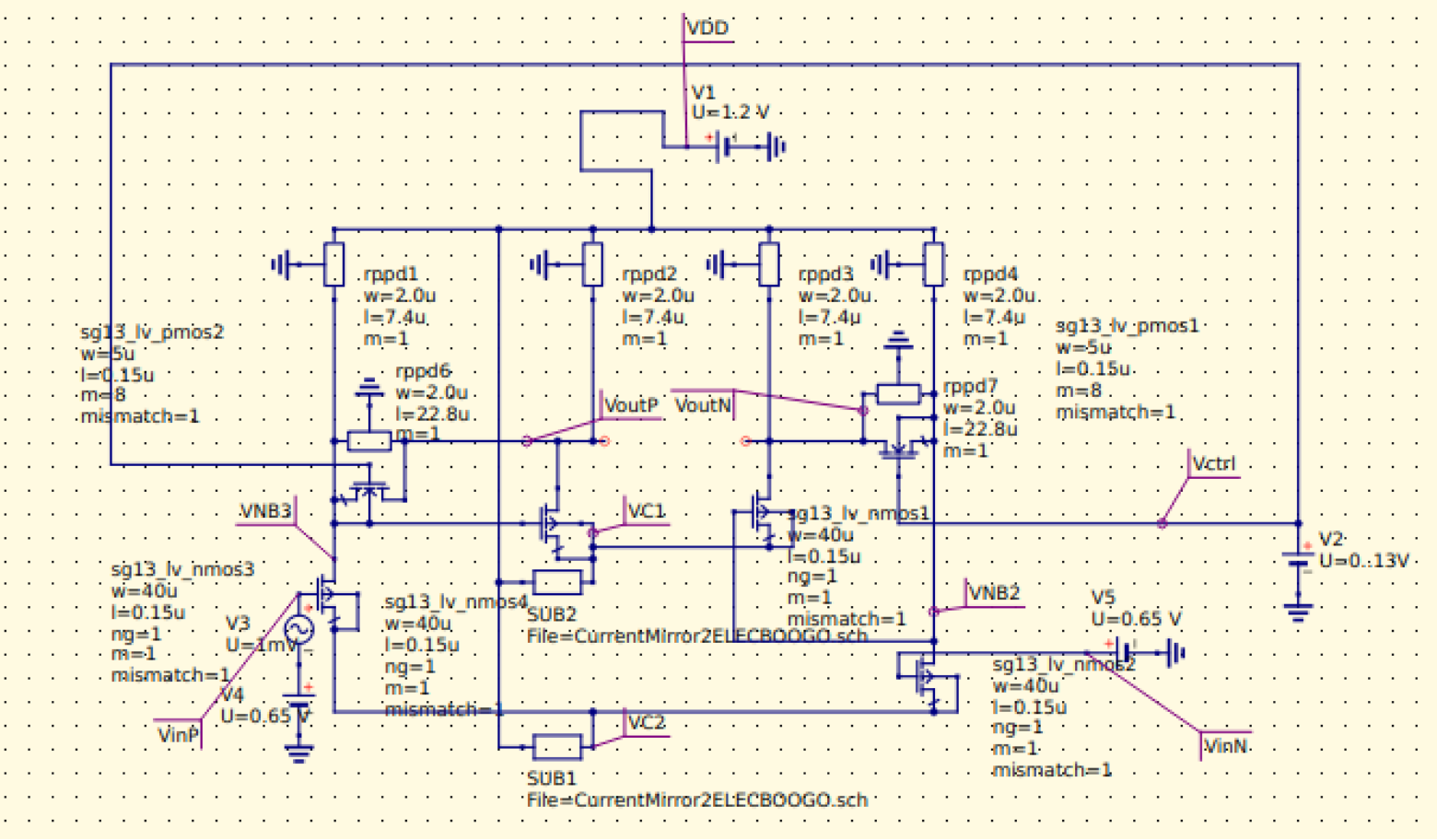
Modified Cherry-Hooper topology





VGA Implementation

Differential gain cell with tunable feedback and two bias branches



DC Operating Point

Reported node voltages at Vctrl = 0 V

Node	DC voltage
VNB2 / VNB3	0.702 V / 0.702 V
VoutN / VoutP	0.702 V / 0.702 V
VC1	0.234 V
VC2	0.185 V

Bias context for the current mirror

VC1 and VC2 sit at 234 mV and 185 mV. These low bias-node voltages make mirror headroom an important design constraint.

Current Mirror Biasing Issue

The mirror must supply the 1mA bias currents at output-node voltages as low as 185 mV

Current-copy error

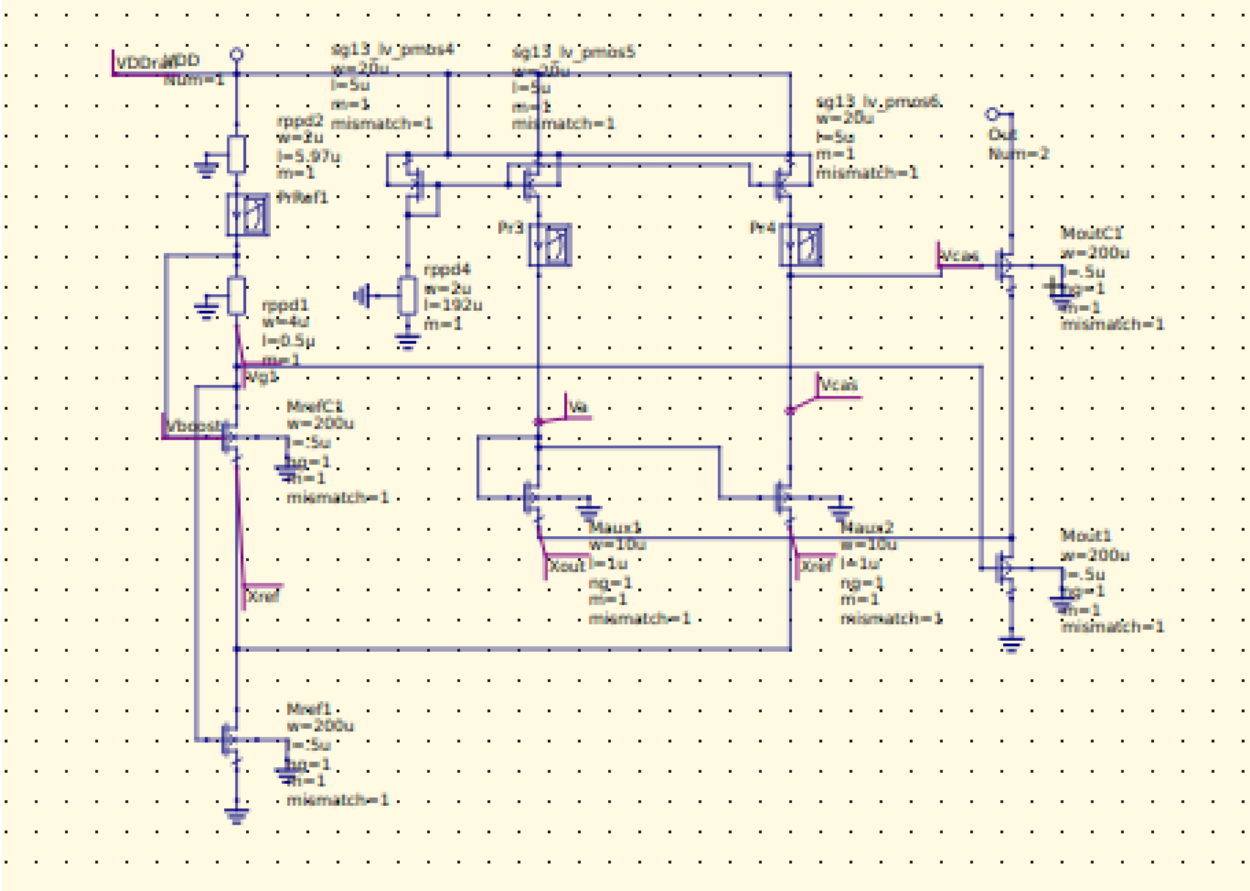
The standard mirror did not maintain the intended bias at these low node voltages. Insufficient saturation margin or unequal reference and output drain voltages can cause current error.

Effect on the VGA

An incorrect bias current shifts the operating point and changes transistor transconductance. Large errors induced that completely ruined performance.

Revised Current Mirror

Separate bias and cascode-control branches



Reference

Establishes the current-copy operating point.

Vcas and Vcasn

Bias the stacked output devices. The design targets a steadier output current at the VGA's DC node voltages.

Related work: V. Michal, "Regulated Cascode Current Mirror with Improved Voltage Swing," AE, 2022.

Mirror Design Tradeoffs

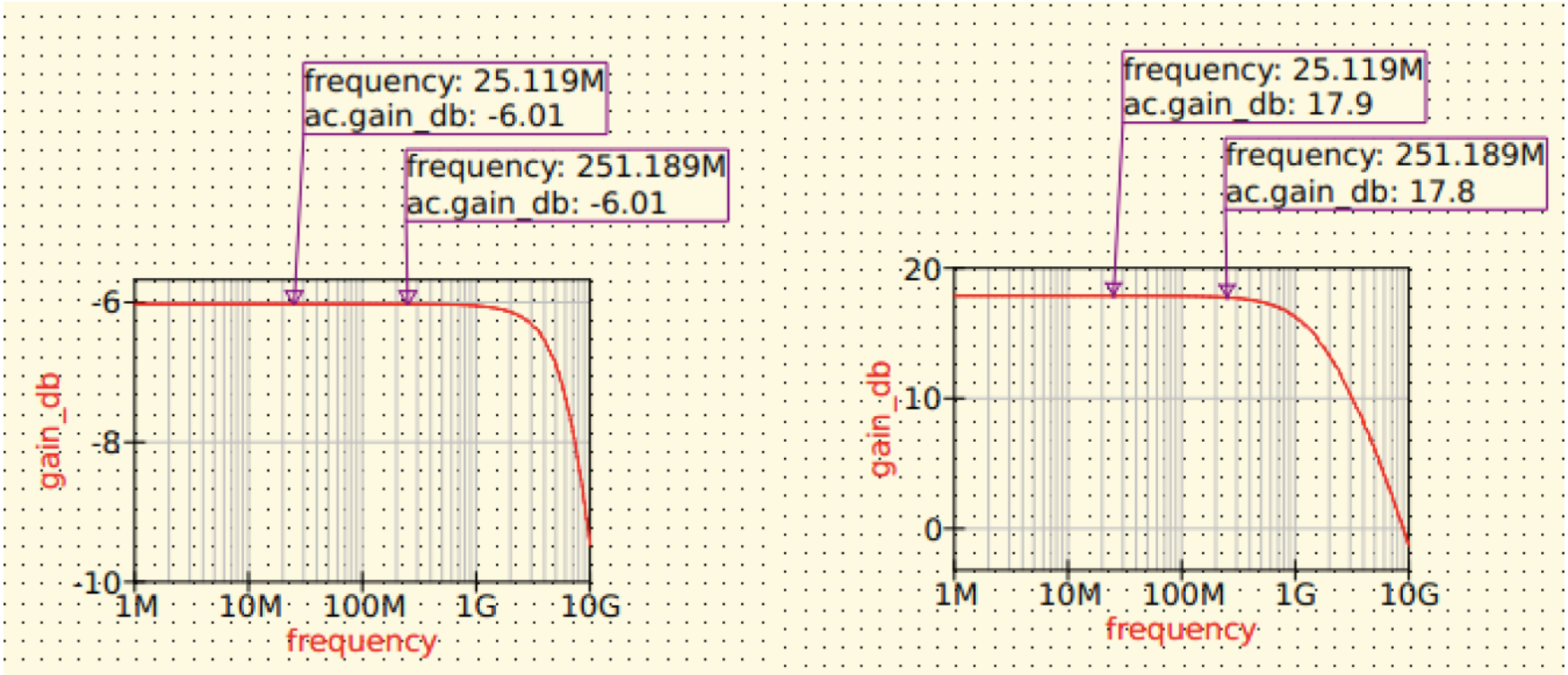
Current accuracy

Cascode action reduces the influence of output-voltage changes on the current-setting device.

Circuit overhead

Extra bias branches consume current and add capacitance. This implementation doubled circuit power consumption.

Gain and Frequency Response

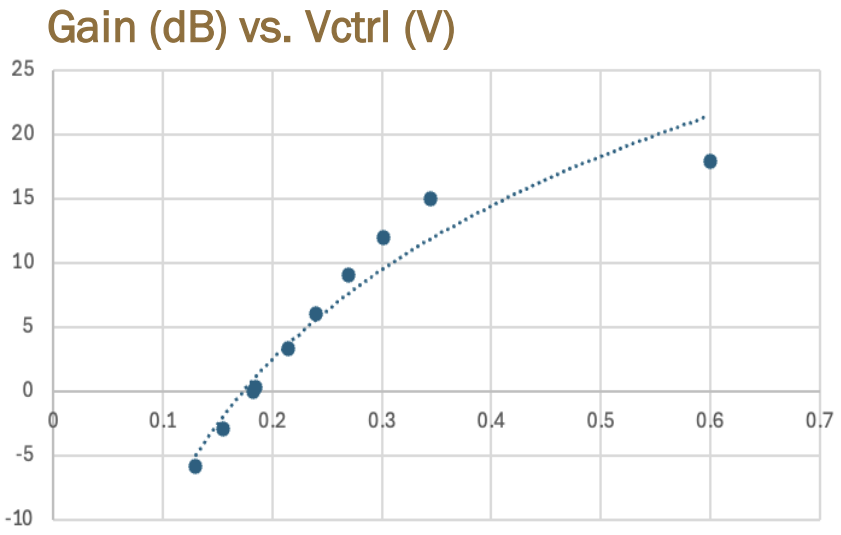


Minimum gain: −6.01 dB

Maximum gain: +17.9 dB

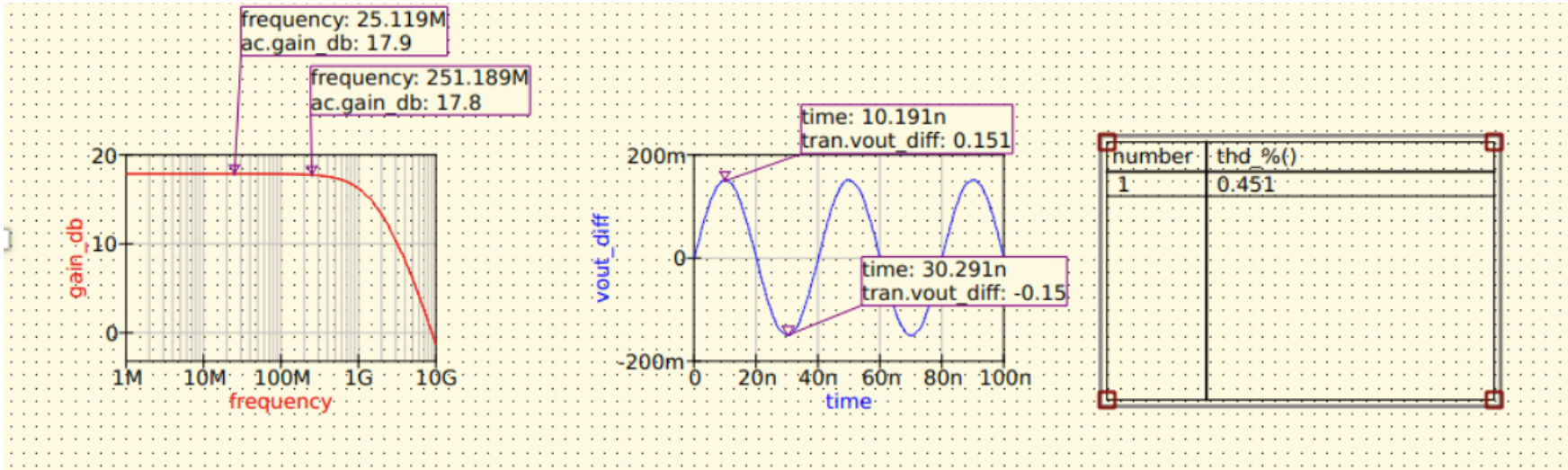
Gain Control and Step Size

Vctrl (V)	Gain (dB)	Step (dB)
0.1285	−6.01	—
0.1300	−5.83	0.18
0.1550	−2.93	2.90
0.1820	0.0193	2.9493
0.1845	0.285	0.2657
0.2140	3.28	2.995
0.2400	6.05	2.67
0.2700	9.05	3.00
0.3020	12.00	2.95
0.3450	15.00	3.00
0.6000	17.90	2.90



Output Swing and Distortion

Maximum-gain transient test at approximately 25 MHz



301 mVpp

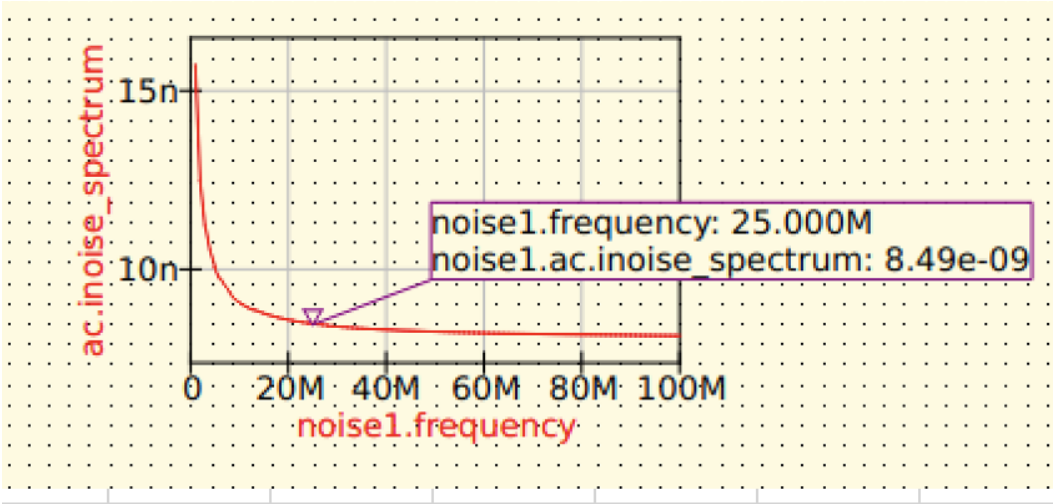
Observed differential output swing

THD = −46.92 dB

11.92 dB below the −35 dB limit

Noise

Noise result and gain-dependent signal limits



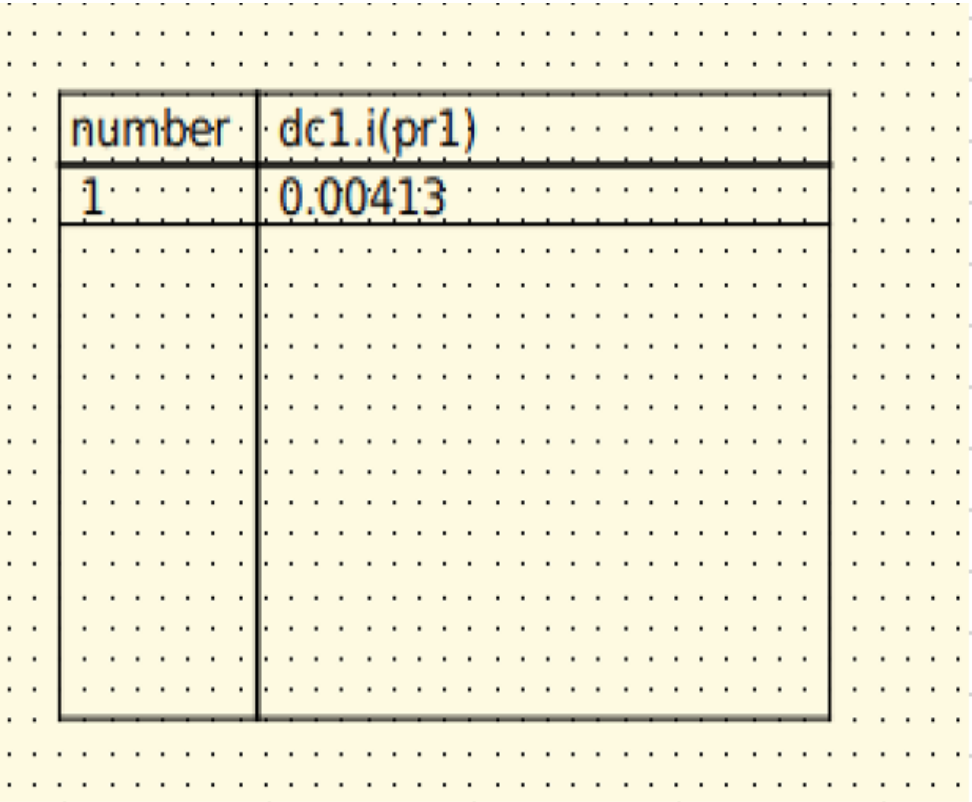
8.49 nV/√Hz

at 25 MHz and Maximum Gain

Below the 15 nV/√Hz

Power Consumption

DC supply-current measurement at 1.2 V



number	dc1.i(pr1)
1	0.00413

4.956 mW

P = VDD × IDD
= 1.2 V × 4.13 mA

Target: < 5 mW
Margin: 0.044 mW (0.88%)

Simulation Results Summary

Comparison with the updated design targets

Metric	Evidence supplied	Assessment
Gain range	−6.01 to +17.9 dB	Near nominal endpoints
Gain step	Maximum listed: 3.095 dB	Exceeds ≤ 3 dB
Bandwidth	Endpoint drop ≤ 0.1 dB at 251.189 MHz	Endpoints supported; other gains unverified
Gain error	Nearest 3 dB nominal setpoint: ≤ 0.38 dB	Within 1.5 dB under this mapping
Output / THD	≈ 301 mVpp / −46.92 dB	Shown test supports swing; verify THD at 250 mVpp
Input noise	8.49 nV/√Hz at 25 MHz	Below limit; confirm maximum-gain setting
Power	1.2 V × 4.13 mA = 4.956 mW	Below 5 mW by 0.044 mW

Design References

Circuit literature and project implementation

VGA topology

C. Fan et al., “Design of a Wideband dB-Linear Variable Gain Amplifier With Continuous Gain Adjusting in 90-nm CMOS Technology,” IEEE Access, vol. 9, pp. 152646–152656, 2021.

doi: 10.1109/ACCESS.2021.3127356

Current-mirror background

V. Michal, “Regulated Cascode Current Mirror with Improved Voltage Swing,” International Conference on Applied Electronics, pp. 125–128, 2022.

doi: 10.1109/AE54730.2022.9920096

Thank You

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